Project profile

Cluster for Application and Technology Research in Europe on NanoElectronics

CT105 | 3D-TSV integration for multimedia and mobile applications (3DIM³)

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	✔
More Moore	
Technology node	

ELECTRONIC DESIGN AUTOMATION FOR ADVANCED SOC AND SIP DESIGN

Partners:

Cadence Design Systems
CEA-LETI
EADS DS
Fraunhofer Institute
Infineon Technologies
Lyon Institute of Nanotechnology
NXP Semiconductors
R3Logic
Recore Systems
STMicroelectronics
TIMA Laboratory
TU Delft
University of Erlangen-Nürnberg
Virage Logic

Project leader:

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Key project dates:

Start: July 2009
End: December 2012

Countries involved:

France
Germany
The Netherlands

The 3DIM³ project intends to provide novel systems-design methodologies, new design tools and systems architectures to handle emerging three-dimensional through silicon via (3D TSV) integration technologies for multimedia and mobile products. The outcome of 3DIM³ will enable the design of 3D TSV integrated multimedia and mobile products with higher performance, lower power consumption and smaller size/form factor, from system and architecture levels to layout, at a lower cost than can currently be achieved. The European partners brought together in this CATRENE project are experts in the design and production of integrated circuits based on system-on-chip and system-in-package technologies.

Three-dimensional (3D) integration is an attractive option for many advanced consumer products. By replacing single-chip packages with 3D devices, higher transistor density and power savings are achieved, data travel distances are shortened and manufacturing costs cut. Key to stacking is the use of through silicon via (TSV) – a chip-assembly technique which impacts the overall electrical and physical design process.

TSV involves making a hole through the wafer on the bottom side – the top side carries the upper metal layer – to reach the first metal layer. The hole is then metallised and connection is made with a redistribution layer to another connection type such as a solder bump. Subsequent thinning of the device wafer bares the metallised TSVs, which are then connected directly or via a redistribution metal layer from the bottom side to a suitable metal layer, such as electroplated copper, for stacking by a soldering technique.

The assembly challenge is to reach the first metal layer in a reliable manner without creating a large hole that would have a profound effect on the die size. Holes are made at wafer level on the reverse side while the hole size depends on the wafer thickness and the techniques applied to make the holes.

Early decision necessary

3D TSV integration also enables the integration of different types of chips and devices in a single package or a compact subsystem, gaining maximum benefit from highly specialised and heterogeneous technologies. However, to take full advantage of 3D integration, the decision must be made early in the architecture planning process rather than as a packaging decision after circuit design is complete. This requires taking 3D design space into account from the start of the system design to distribute its different parts into a new set of chips that will be stacked.

So far, huge investments have been made in fabrication to deliver these technologies but few results exist in terms of design methods and tools. The capacity to design, build and validate 3D products is likely to become the next enabler of further silicon integration.

The CATRENE CT105 3DIM³ project is tackling the challenges for the development of 3D TSV integration technologies for future multimedia and mobile systems. It will provide the design methods and tools that make the best trade-off between system partitioning and cost, at the same time focusing on a novel 3D TSV integration packaging approach.

Technology partitioning

The market success of 3D TSV products can be guaranteed if three challenges are correctly addressed:

1. The required performance must be provided at a reasonable power;
2. The cost per function must be reduced; and

3. The development must be carried out in the right time frame at reasonable design and manufacturing cost.

Analysing the requirements and the potential system architecture solutions of multimedia and mobile applications indicates that computing performance will be in the order of Tera-operations/s. It will also certainly be addressed by multi-core architectures – from tens to several tens of cores – thanks to the capabilities provided by technologies of 32 nm and beyond.

However, issues remain to be solved in the memory hierarchy and its throughput. The best chip-level system partitioning trade-off should be made for performance in terms of computing power, memory throughput, power consumption, size and form factor versus cost on- or off-chip.

Handling heterogeneous elements

Apart from computing power, crucial elements contributing to the success of these future applications will be the ability of the device to manage heterogeneous elements such as digital, analogue, radio frequency (RF), discrete devices – resistors, inductances and capacitors – and software.

Analogue and RF components do not have the same capacity for downscaling as digital logic. Even worse, the size of the analogue and RF components could increase when scaling down the technology. Again, the best system partitioning for chip-level trade-off would be technology versus cost on- or off-chip.

Input/output and analogue circuits – about 40% of the original device – only scale at about half the rate of digital logic, losing an order of magnitude in dice/wafer size over several process generations as the dice does not scale as easily as digital transistors. By partitioning the different layers of silicon, 3DIM³ will overcome this limitation, allowing designers to get the best of each technology.

The physical characteristics of the packaging should also be considered, such as throughput, power consumption, thermal, size and form factor as well as electrical in terms of voltage, signal integrity.

Drastic improvement

3DIM³ aims to provide 3D TSV design solutions to improve the multimedia and mobile product design process in terms of quality and productivity. The design solutions proposed represent a pioneering approach to the design of 3D TSV silicon integration technologies.

The potential benefits of 3D integration include multi-functionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration and reduced overall costs. The main contribution will be a drastic improvement of the system-on-chip (SoC) design process in terms of quality and productivity.

Four key innovations will enable 3DIM³ to bridge the gap between SoC applications and design methods:

1. ***System re-architecture breakthrough:*** design approaches including 3D partitioning at geometry, technology and functional levels to select the best cost/performance trade-offs;
2. ***3D system-architecture breakthrough:*** better 3D system architecture, design methods and tools and components such as interconnects, analogue and RF;
3. ***3D design-automation breakthrough:*** upgrade the design flow to handle 3D design; and
4. ***Linking fabrication process to system-level design breakthrough***: design for novel silicon integration and packaging approaches to master 3D solutions.

The innovative 3D design solutions from this CATRENE project will enable European multimedia and mobile device manufacturers to maintain leadership in this strategic market by increasing the ability of their designers to build larger and better quality systems in less time and at lower cost. More powerful 3D SoC/system-in-package devices and the increasing complexity of managing the 3D products will drive widespread adoption of 3D design method solutions for mobile and multimedia product designs.

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

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